Refine Search

Search Results -

Term	Documents
(5 AND 2).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	48
(L2 AND L5).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	48

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L14

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DATE: Monday, July 19, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L14	l2 and l5	48	L14
L13	l2 and l4	52	L13
L12	l6 and @py<=1991	1	L12
L11	l2 and @py<=1991	4	L11
L10	l3 and l5	3	L10
L9	L3 and l4	3	L9
L8	l5 and L6	20	L8
L7	l4 and L6	22	L7
L6	(dsp or digital near1 signal) near8 (one or single) near4 (instruction$1 or command$1) near25 general near3 purpose	31	L6
DB=PGPB,USPT; PLUR=YES; OP=OR			
L5	(712/35-36)![CCLS]	394	L5

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L4	(712/30-39)![CCLS]	1380	L4
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L3	(dsp or digital near1 signal) near8 (one or single) near4 (instruction$1 or command$1) near25 general near3 purpose near3 (process$3 or microprocess$3)	7	L3
L2	(dsp or digital near1 signal) near8 (one or single) near4 (instruction$1 or command$1) and general near3 purpose near3 (process$3 or microprocess$3)	243	L2
L1	(dsp or digital near1 signal) near8 (one or single) near4 (instruction$1 or command$1)	1067	L1

END OF SEARCH HISTORY

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(dsp or digital signal) and general purpose and single | Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

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1 **A low-cost media-processor based real-time MPEG-4 video decoder**
Jin-Hau Kuo; Chia-Chiang Ho; Kan-Li Huang; Jim Shiu; Ja-Ling Wu;
Consumer Electronics, IEEE Transactions on , Volume: 49 , Issue: 4 , Nov. 2C
Pages:1488 - 1497

[Abstract] [PDF Full-Text (556 KB)] **IEEE JNL**

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2 **Real-time software based MPEG-4 video encoder**
Weiguo Zheng; Ahmad, I.; Liou, M.L.;
MPEG-4. 2001 Proceedings of Workshop and Exhibition on , 18-20 June 2001
Pages:71 - 74

[Abstract] [PDF Full-Text (405 KB)] **IEEE CNF**

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3 **Some fast speech processing algorithms using AltiVec technology**
Joshi, S.M.; Dubey, P.K.;
Acoustics, Speech, and Signal Processing, 1999. ICASSP '99. Proceedings., 1
IEEE International Conference on , Volume: 4 , 15-19 March 1999
Pages:2135 - 2138 vol.4

[Abstract] [PDF Full-Text (312 KB)] **IEEE CNF**

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4 **A 51.2-GOPS scalable video recognition processor for intelligent cru control based on a linear array of 128 four-way VLIW processing elen**
Kyo, S.; Koga, T.; Okazaki, S.; Kuroda, I.;
Solid-State Circuits, IEEE Journal of , Volume: 38 , Issue: 11 , Nov. 2003
Pages:1992 - 2000

[Abstract] [PDF Full-Text (832 KB)] **IEEE JNL**

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5 **Subword extensions for video processing on mobile systems**
Jennings, M.D.; Coate, T.M.;
Concurrency, IEEE [see also IEEE Parallel & Distributed Technology] , Volume 6 , Issue: 3 , July-Sept. 1998
Pages:13 - 16

[Abstract] [PDF Full-Text (140 KB)] IEEE JNL

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6 **A programmable digital filter IC employing multiple processors on a single chip**
Kwentus, A.Y.; Werter, M.J.; Willson, A.N., Jr.;
Circuits and Systems for Video Technology, IEEE Transactions on , Volume: 2 , Issue: 2 , June 1992
Pages:231 - 244

[Abstract] [PDF Full-Text (1056 KB)] IEEE JNL

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7 **Short vector code generation and adaptation for DSP algorithms**
Franchetti, F.; Puschel, M.;
Acoustics, Speech, and Signal Processing, 2003. Proceedings. (ICASSP '03). 2
IEEE International Conference on , Volume: 2 , 6-10 April 2003
Pages:II - 537-40 vol.2

[Abstract] [PDF Full-Text (366 KB)] IEEE CNF

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8 **SVP: scan-line video processor-general purpose video processor**
Onuma, H.; Yaguchi, Y.; Miyaguchi, H.; Akiyama, T.; Kajiyama, K.; Adachi, K Kikuchi, A.; Kojima, T.; Narumi, T.;
VLSI Technology, Systems, and Applications, 1995. Proceedings of Technical Papers., 1995 International Symposium on , 31 May-2 June 1995
Pages:196 - 200

[Abstract] [PDF Full-Text (268 KB)] IEEE CNF

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9 **Efficient FFT implementation on an IEEE floating-point digital signal processor**
Kloker, K.L.; Lindsley, B.; Baron, N.; Sohie, G.R.L.;
Acoustics, Speech, and Signal Processing, 1989. ICASSP-89., 1989 Internatio Conference on , 23-26 May 1989
Pages:1302 - 1305 vol.2

[Abstract] [PDF Full-Text (312 KB)] IEEE CNF

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Search Results - Record(s) 1 through 16 of 16 returned.

☐ 1. Document ID: US 6353863 B1

L10: Entry 1 of 16 File: USPT Mar 5, 2002

US-PAT-NO: 6353863
DOCUMENT-IDENTIFIER: US 6353863 B1

TITLE: Terminal

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. Desc | Image

☐ 2. Document ID: US 6260088 B1

L10: Entry 2 of 16 File: USPT Jul 10, 2001

US-PAT-NO: 6260088
DOCUMENT-IDENTIFIER: US 6260088 B1
**** See image for Certificate of Correction ****

TITLE: Single integrated circuit embodying a risc processor and a digital signal processor

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. Desc | Image

☐ 3. Document ID: US 5872960 A

L10: Entry 3 of 16 File: USPT Feb 16, 1999

US-PAT-NO: 5872960
DOCUMENT-IDENTIFIER: US 5872960 A

TITLE: Integrated circuit having CPU core operable for switching between two independent asynchronous clock sources of different frequencies while the CPU continues executing instructions

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw. Desc | Image

☐ 4. Document ID: US 5685005 A

L10: Entry 4 of 16 File: USPT Nov 4, 1997

US-PAT-NO: 5685005
DOCUMENT-IDENTIFIER: US 5685005 A

TITLE: Digital signal processor configured for multiprocessing

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw. Desc | Image

☐ 5. Document ID: US 5649208 A

L10: Entry 5 of 16 File: USPT Jul 15, 1997

US-PAT-NO: 5649208
DOCUMENT-IDENTIFIER: US 5649208 A

TITLE: Mechanism for handling non-maskable interrupt requests received from different sources

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw. Desc | Image

☐ 6. Document ID: US 5630153 A

L10: Entry 6 of 16 File: USPT May 13, 1997

US-PAT-NO: 5630153
DOCUMENT-IDENTIFIER: US 5630153 A

TITLE: Integrated digital signal processor/general purpose CPU with shared internal memory

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw. Desc | Image

☐ 7. Document ID: US 5613149 A

L10: Entry 7 of 16 File: USPT Mar 18, 1997

US-PAT-NO: 5613149
DOCUMENT-IDENTIFIER: US 5613149 A

TITLE: Integrated data processing system utilizing successive approximation analog to digital conversion and PWM for parallel disconnect

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw. Desc | Image

☐ 8. Document ID: US 5611075 A

L10: Entry 8 of 16 File: USPT Mar 11, 1997

US-PAT-NO: 5611075

DOCUMENT-IDENTIFIER: US 5611075 A

TITLE: Bus architecture for digital signal processor allowing time multiplexed access to memory banks

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw. Desc | Image

☐ 9. Document ID: US 5606714 A

L10: Entry 9 of 16 File: USPT Feb 25, 1997

US-PAT-NO: 5606714
DOCUMENT-IDENTIFIER: US 5606714 A

TITLE: Integrated data processing system including CPU core and parallel, independently operating DSP module and having multiple operating modes

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw. Desc | Image

☐ 10. Document ID: US 5603017 A

L10: Entry 10 of 16 File: USPT Feb 11, 1997

US-PAT-NO: 5603017
DOCUMENT-IDENTIFIER: US 5603017 A

TITLE: Parallel integrated circuit having DSP module and CPU core operable for switching between two independent asynchronous clock sources while the system continues executing instructions

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw. Desc | Image

☐ 11. Document ID: US 5592677 A

L10: Entry 11 of 16 File: USPT Jan 7, 1997

US-PAT-NO: 5592677
DOCUMENT-IDENTIFIER: US 5592677 A
**** See image for Certificate of Correction ****

TITLE: Integrated data processing system including CPU core and parallel, independently operating DSP module

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw. Desc | Image

☐ 12. Document ID: US 5590357 A

L10: Entry 12 of 16 File: USPT Dec 31, 1996

US-PAT-NO: 5590357
DOCUMENT-IDENTIFIER: US 5590357 A
**** See image for Certificate of Correction ****

TITLE: Integrated CPU core and parallel, independently operating DSP module and time-critical core priority scheme

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw. Desc | Image

☐ 13. Document ID: US 5519879 A

L10: Entry 13 of 16 File: USPT May 21, 1996

US-PAT-NO: 5519879
DOCUMENT-IDENTIFIER: US 5519879 A

TITLE: Integrated circuit having CPU and DSP for executing vector lattice propagation instruction and updating values of vector Z in a single instruction cycle

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw. Desc | Image

☐ 14. Document ID: US 5511219 A

L10: Entry 14 of 16 File: USPT Apr 23, 1996

US-PAT-NO: 5511219
DOCUMENT-IDENTIFIER: US 5511219 A

TITLE: Mechanism for implementing vector address pointer registers in system having parallel, on-chip DSP module and CPU core

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw. Desc | Image

☐ 15. Document ID: US 5491828 A

L10: Entry 15 of 16 File: USPT Feb 13, 1996

US-PAT-NO: 5491828
DOCUMENT-IDENTIFIER: US 5491828 A

TITLE: Integrated data processing system having CPU core and parallel independently operating DSP module utilizing successive approximation analog to digital and PWM for parallel disconnect

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw. Desc | Image

☐ 16. Document ID: US 5487173 A

L10: Entry 16 of 16 File: USPT Jan 23, 1996

US-PAT-NO: 5487173
DOCUMENT-IDENTIFIER: US 5487173 A

TITLE: DTMF detection in an integrated data processing system

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw. Desc | Image

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Term	Documents
(9 AND 3).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	16
(L3 AND L9).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	16

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